MMBF0202PLT1

Preferred Device

Power MOSFET 300 mAmps, 20 Volts

P−Channel SOT−23

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in small power management circuitry. Typical applications are dc−dc converters, power management in portable and battery−powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

Features

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SOT−23 Surface Mount Package Saves Board Space
- Pb−Free Package is Available

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	20	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	± 20	Vdc
Drain Current − Continuous @ T_A = 25°C − Continuous @ T_A = 70°C − Pulsed Drain Current ($t_p \le 10$ μs)	 I_D I_D I_{DM}	 300 240 750	mAdc
Total Power Dissipation @ T_A = 25°C (Note 1)	P_D	225	mW
Operating and Storage Temperature Range	T_J, T_{stg}	− 55 to 150	°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	625	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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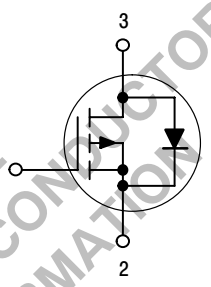
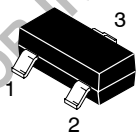
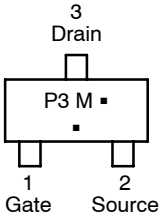
300 mAMPS, 20 VOLTS
$R_{DS(on)}$ = 1.4 Ω

P−Channel



MARKING DIAGRAM AND PIN ASSIGNMENT





SOT−23
CASE 318
STYLE 21

P3 = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MMBF0202PLT1	SOT−23	3000 Tape & Reel
MMBF0202PLT1G	SOT−23 (Pb−Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μA)		$V_{(BR)DSS}$	20	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 16 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	– –	– –	1.0 10	μAdc
Gate−Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	–	–	±100	nAdc
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	1.7	2.4	Vdc
Static Drain−to−Source On−Resistance (V_{GS} = 10 Vdc, I_D = 200 mAdc) (V_{GS} = 4.5 Vdc, I_D = 50 mAdc)		$r_{DS(on)}$	– –	0.9 2.0	1.4 3.5	Ω
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 200 mAdc)		g_{FS}	–	600	–	mMhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 5.0 V)	C_{iss}	–	50	–	pF
Output Capacitance	(V_{DS} = 5.0 V)	C_{oss}	–	45	–	
Transfer Capacitance	(V_{DG} = 5.0 V)	C_{rss}	–	20	–	
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	(V_{DD} = −15 Vdc, R_L = 75 Ω, I_D = 200 mAdc, V_{GEN} = −10 V, R_G = 6.0 Ω)	$t_{d(on)}$	–	2.5	–	ns
Rise Time		t_r	–	1.0	–	
Turn−Off Delay Time		$t_{d(off)}$	–	16	–	
Fall Time		t_f	–	8.0	–	
Gate Charge (See Figure 5)	(V_{DS} = 16 V, V_{GS} = 10 V, I_D = 200 mA)	Q_T	–	2700	–	pC
SOURCE−DRAIN DIODE CHARACTERISTICS						
Continuous Current		I_S	–	–	0.3	A
Pulsed Current		I_{SM}	–	–	0.75	
Forward Voltage (Note 3)		V_{SD}	–	1.5	–	V

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

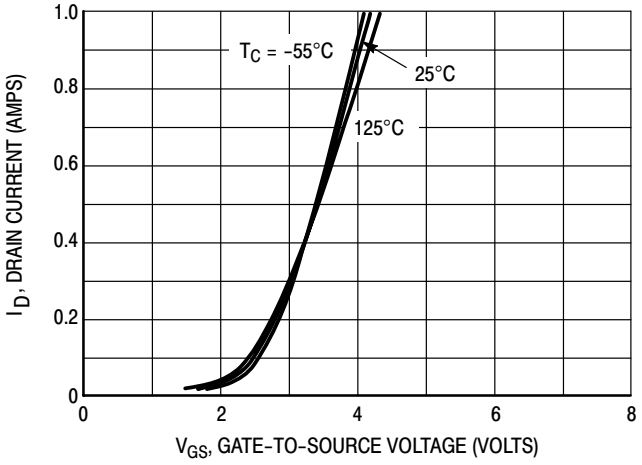


Figure 1. Transfer Characteristics

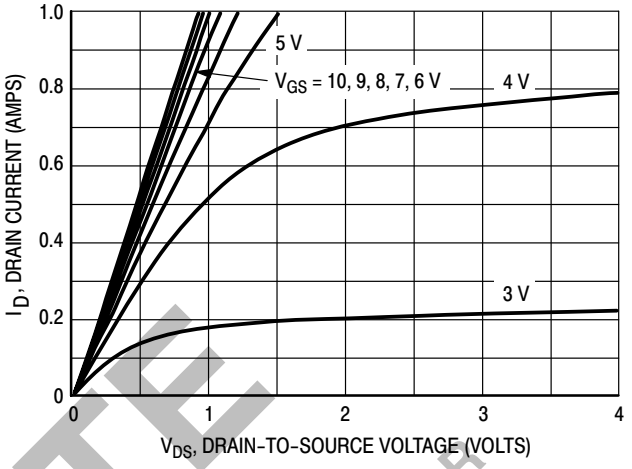


Figure 2. On−Region Characteristics

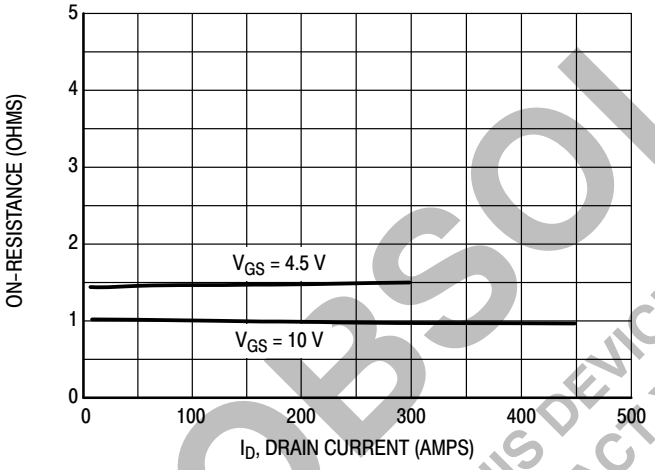


Figure 3. On−Resistance versus Drain Current

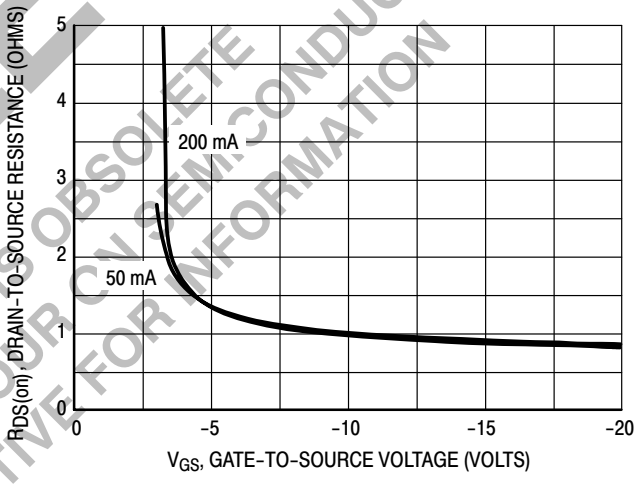


Figure 4. On−Resistance versus Gate−to−Source Voltage

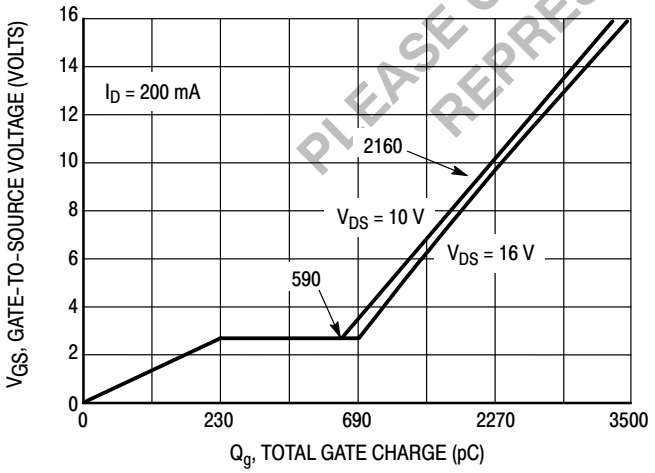


Figure 5. Gate Charge

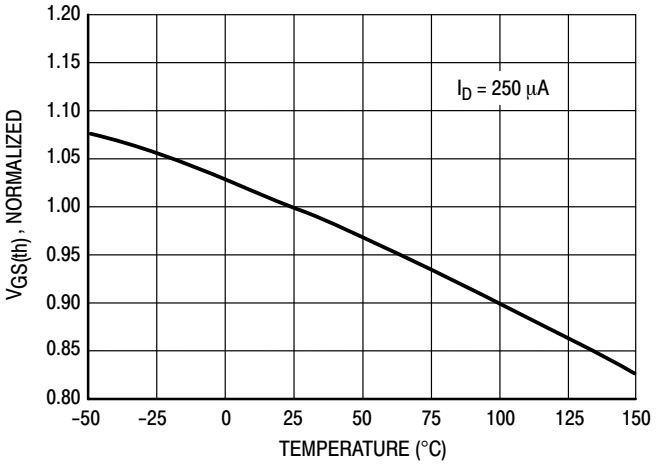


Figure 6. Threshold Voltage Variance Over Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

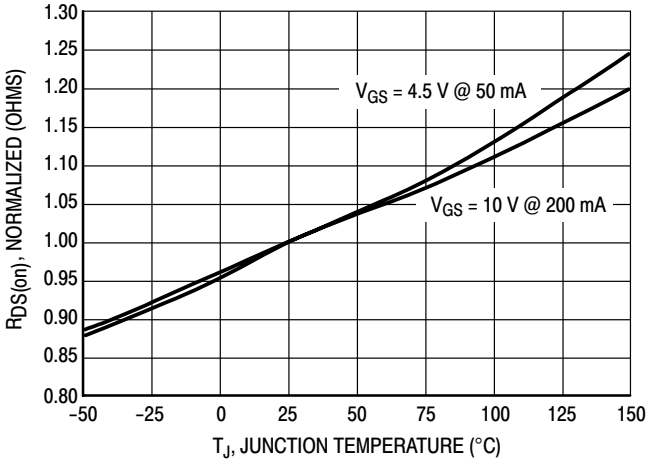


Figure 7. On−Resistance versus Junction Temperature

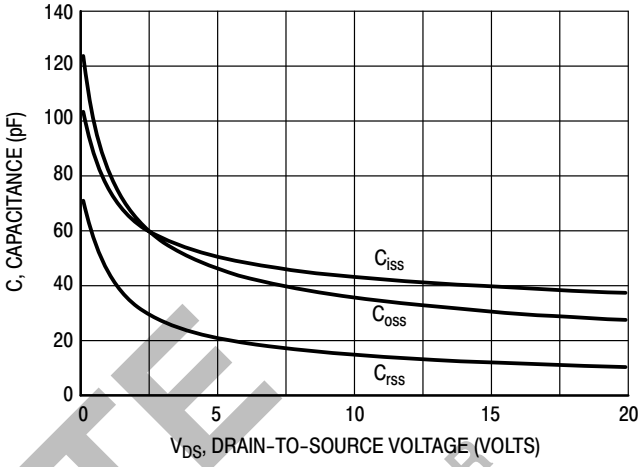


Figure 8. Capacitance

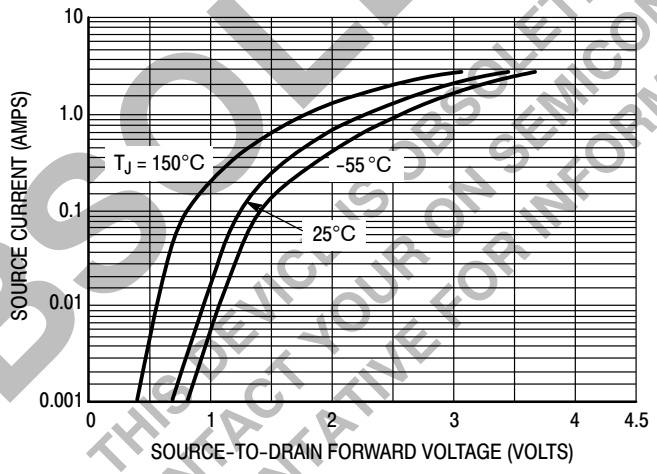
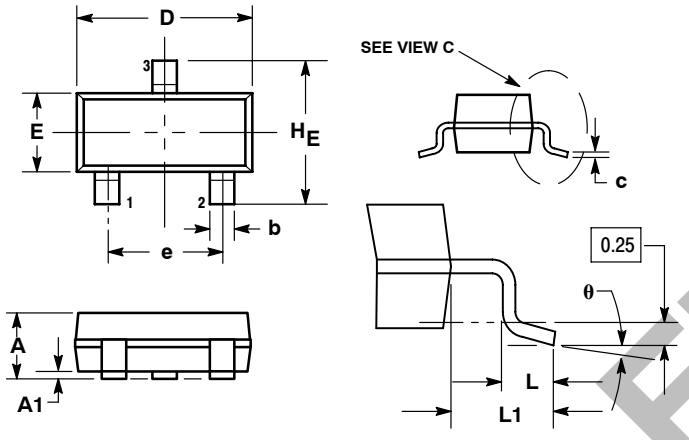


Figure 9. Source−to−Drain Forward Voltage versus Continuous Current (I_S)

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AN

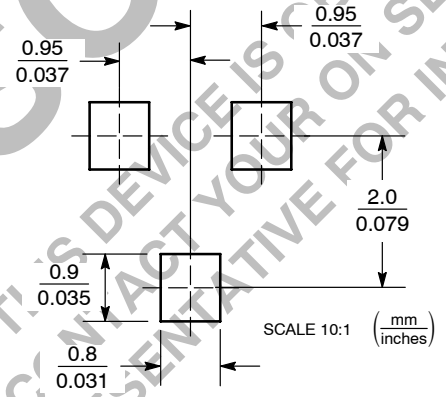


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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